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A2

16. (Amended) The method of claim 14 including the steps as follows:

forming the metal vias by forming a blanket through via/cap pad layer of a first metal layer over dielectric layer including the via holes,

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming the metal vias in the via holes,

then forming the interconnection structure over the first surface including the metal vias and the first metal layer,

then forming the temporary bond to a rigid wafer holder on the reverse surface, and

then thinning the wafer to the desired thickness of the UTSW.

## REMARKS

The claims have been amended in view of the Office action and in view of the remarks which follow, they are believed to be in condition for allowance.

## Restrictions

In the Office Action, restriction was required under 35 U.S.C. 121 to one of the inventions. The Office Action stated as follows:

> "I. Claims 1-16 drawn to process, classified in class 438, subclass 106."
> "II. Claims 17-24, drawn to device, classified in class 257, subclass 678."
> "The inventions are distinct, each from the other because of the following reasons:
> "Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process. For example, without a temporary bonding step."
> "Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper."

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The requirement for restriction is traversed.

It is respectfully submitted that it is believed that because the above argument, is very general, it may have been be based upon speculation that cannot be supported by a detailed analysis. In the absence of a detailed explanation and analysis, it is not seen how the product could be made without the temporary bonding step since that is an integral feature of the instant invention. Thus, it is believed that the requirement for restriction should be withdrawn and that the device claims should be examined along with the method claims. Most of the features in the process and device claims are very similar and the subject matter of the claims is integrally intertwined Thus, it is believed that, in order to be complete, a search would need to be made in both classes and subclasses. For that reason, it is respectfully submitted that it is believed no substantial additional burden of searching to be required. Accordingly, it is respectfully requested that the Requirement for Restriction be withdrawn.

The Office Action stated further as follows:

"Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143)."

As stated above, the method claims 1-16 are provisionally elected for examination with traverse.

Attached hereto is a version of amendments to the specification and/or claims with markings to show changes made.

In view of the amendments and the above remarks favorable action including allowance of the claims and the application as a whole are respectfully solicited.

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Respectfully submitted,

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

## IN THE CLAIMS

**Please amend the claims as follows:**

**1. (Amended) A method [ ~~for fabricating a silicon based package (SBP)~~ ] comprising:**

**starting [start] with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for a silicon based package (SBP) [~~the SBP~~],**

**forming an interconnection structure including multilayer conductor patterns over the first surface,**

**forming a temporary bond between the SBP and a wafer holder, with the wafer holder being a rigid structure,**

**thinning the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP,**

**forming via holes which extend through the UTSW, and**

**forming metallization in the via holes with the metallization extending through the UTSW.**

**14. (Amended) A method [~~for fabricating a silicon based package (SBP)~~] comprising:**

**providing a base for a silicon based package (SBP) [~~the SBP~~] comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,**

**forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,**

**forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,**

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forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

forming an interconnection structure including multilayer conductor patterns over the metal vias and the dielectric layer,

forming a temporary bond between the SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

thinning the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, and

removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW.

15. (Amended) The method of claim 14 including the steps [of] <u>as follows:</u>

forming the metal vias by forming a blanket through via/cap pad layer of a first metal layer over dielectric layer including the via holes,

followed by planarizing the via/cap pad layer down to the surface of the dielectric layer, thereby forming the metal vias in the via holes.

16. (Amended) The method of claim 14 including the steps [of] <u>as follows:</u>

forming the metal vias by forming a blanket through via/cap pad layer of a first metal layer over dielectric layer including the via holes,

[~~followed by~~] <u>then</u> planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming the metal vias in the via holes,

then forming the interconnection structure over the first surface including the metal vias and the first metal layer,

then forming the temporary bond to a rigid wafer holder on the reverse surface, and

then thinning the wafer to the desired thickness of the UTSW.